ADAPTIVE PHASE LOCKED LOOP

ABSTRACT OF THE DISCLOSURE

A reference signal and a voltage controlled oscillator (VCO) output are compared for relative phase and frequency differences. A lead error signal is generated if the reference signal leads the VCO output and a lag error signal is generated if the reference signal lags the VCO output the lead and lag error may result from a combination for phase and frequency differences between the reference signal and the VCO output. A time window is used to sample the polarity of the lead and lag error signals by incrementing and decrementing a phase error signal. If the phase error signal reaches a threshold value within the time window, a Reset Delta pulse is generated and if the phase error signals does not reach the maximum delta value within the time window a Reset Total pulse is generated. A variable first gain signal is increased on each Reset Delta pulse and decreased on each Reset Total pulse and limited to a value between predetermined maximum and minimum values. The first gain signal is multiplied by a Pump current increment and added to a minimum Pump current to generate a variable Pump current. A variable second gain signal proportional to the time the reference signal leads and lags the VCO signal multiplies the Pump current. The amplified Pump current is summed with an integral of the amplified Pump current to generate a control signal. The control signal is applied to the VCO and determines the frequency of the VCO output.